

**What is claimed is:**

- 1     1.     A method for analyzing a semiconductor die having circuitry in a circuit side  
2     opposite a back side, the method comprising:  
3         applying an electric field to the die via a voltage-application tool, separate from  
4     the die and using the applied electric field to stimulate circuitry in the die;  
5         detecting a response of die to the applied electric field; and  
6         using the response to detect an electrical characteristic from the die.
- 1     2.     The method of claim 1, wherein applying an electric field includes applying an  
2     electric field to circuitry via a die passivation layer in a conventionally packaged  
3     semiconductor die.
- 1     3.     The method of claim 1, wherein applying an electric field includes applying an  
2     electric field to circuitry via a backside of a flip-chip packaged die.
- 1     4.     The method of claim 3, wherein applying an electric field to circuitry via a  
2     backside of a flip-chip packaged die includes applying an electric field via a thinned  
3     backside of the flip-chip packaged die.
- 1     5.     The method of claim 4, further comprising thinning the backside of the flip-chip  
2     packaged die and thereby forming the thinned backside.

1 6. The method of claim 1, wherein applying an electric field includes applying an  
2 electric field to circuitry via an insulator portion of silicon-on-insulator structure in a  
3 die.

1 7. The method of claim 6, further comprising thinning a portion of the die and  
2 exposing the insulator portion of the silicon-on-insulator structure, wherein applying an  
3 electric field to circuitry via the insulator portion includes applying the electric field via  
4 the exposed insulator portion.

1 8. The method of claim 1, wherein applying the electric field includes using at least  
2 one of: a scanning probe microscope, and atomic force microscope and a capacitance  
3 probe microscope.

1 9. The method of claim 1, wherein applying an electric field to the die includes  
2 positioning a probe tip over a portion of circuitry in the die and applying a voltage to  
3 the probe tip.

1 10. The method of claim 9, wherein applying a voltage to the probe tip includes  
2 applying a voltage that varies over time to the probe tip.

1 11. The method of claim 9, wherein detecting a response of the die to the applied  
2 electric field includes detecting a position of the probe tip over the die and mapping the  
3 detected response to circuitry in the die below the probe tip.

1 12. The method of claim 9, wherein positioning the probe tip includes scanning the  
2 probe tip over the die.

1 13. The method of claim 12, wherein detecting a response of the die includes  
2 detecting responses from a plurality of circuits in the die as the probe tip is scanned over  
3 the circuits.

1 14. The method of claim 9, wherein applying a voltage to the probe tip includes  
2 applying a periodic voltage that is relative to a voltage at a reference node in the die.

1 15. The method of claim 9, wherein positioning a probe tip includes positioning a  
2 probe tip having a radius that is sufficiently small to stimulate a selected node in the die  
3 without necessarily stimulating circuitry adjacent to the selected node.

1 16. The method of claim 9, wherein positioning a tip over a portion of circuitry in  
2 the die includes positioning the tip using nanometer-level resolution.

1 17. The method of claim 1, wherein applying an electric field includes applying the  
2 electric field to circuitry via an opaque layer in the die, the circuitry being buried in the  
3 die below the opaque layer.

1 18. The method of claim 1, further comprising using the detected electrical  
2 characteristic to provide a modified die design and manufacturing a semiconductor  
3 device using the modified die design.

1 19. A semiconductor device manufactured using the modified die design of  
2 claim 18.

1 20. The method of claim 1, further comprising using the detected electrical  
2 characteristic to modify a manufacturing process for the die and subsequently using the  
3 modified manufacturing process to manufacture additional dies.

1 21. A method for analyzing and repairing a semiconductor die having silicon-on-  
2 insulator structure, the method comprising:  
3 applying an electric field to the die via the insulator portion of the SOI structure  
4 using a probe tip and using the applied electric field to switch a non-functioning  
5 transistor in the die between a passing state and a blocking state;  
6 detecting the switching of the non-functioning transistor and identifying the  
7 location of the non-functioning transistor as a function of the location of the probe tip  
8 when the switching is detected; and  
9 repairing the non-functioning transistor.

1    22.    The method of claim 21, wherein using the applied electric field to switch a non-  
2    functioning transistor includes switching a transistor having at least one of: an oxide  
3    short and an open gate.

1    23.    The method of claim 21, wherein repairing the non-functioning transistor  
2    comprises depositing a gate on the SOI structure at the location of the probe tip when  
3    the non-functioning transistor is switched, the gate being adapted to switch the  
4    transistor between a passing state and a blocking state.

1    24.    The method of claim 23, further comprising electrically coupling the gate to  
2    other circuitry in the die.

1    25.    The method of claim 23, further comprising:  
2            re-applying an electric field to the die via the insulator portion of the SOI  
3    structure using a probe tip and using the applied electric field to switch a second non-  
4    functioning transistor in the die between a passing state and a blocking state; and  
5            detecting the switching of the second non-functioning transistor and identifying  
6    the location of the second non-functioning transistor as a function of the location of the  
7    probe tip when the switching is detected.

1    26.    The method of claim 23, wherein depositing a gate includes using a focused ion  
2    beam (FIB) to deposit a gate.

1 27. The method of claim 21, after repairing the non-functioning transistor, further  
2 comprising:

3 applying an electric field to the die and using the applied electric field to  
4 stimulate circuitry in the die;

5 detecting a response of die to the applied electric field; and

6 using the response to detect an electrical characteristic of the die.

1 28. A system for analyzing a semiconductor die having circuitry in a circuit side  
2 opposite a back side, the system comprising:

3 means, separate from the die and adapted for applying an electric field to the die

4 and using the applied electric field to stimulate circuitry in the die;

5 means for detecting a response of die to the applied electric field; and

6 means for using the response to detect an electrical characteristic of the die.

1 29. A system for analyzing a semiconductor die having circuitry in a circuit side  
2 opposite a back side, the system comprising:

3 a probe tip arrangement, separate from the die and adapted for applying an

4 electric field to the die for stimulating circuitry in the die;

5 electrical detection circuitry adapted for detecting a response of die to the  
6 applied electric field; and

7 a computer arrangement adapted for using the response to detect an electrical  
8 characteristic of the die.

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- 1 30. The system of claim 29, wherein the probe tip is sufficiently small to apply an
- 2 electric field to stimulate a selected circuit node in the die without necessarily
- 3 stimulating surrounding circuitry in the die.